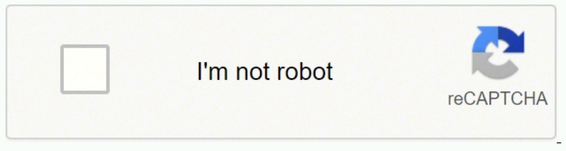

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What is the relation between the ON-resistance of MOSFET and gate to source voltage (Vgs)?ON-resistance linearly increases with Vgs.ON-resistance linearly decreases with Vgs.ON-resistance exponentially increases with Vgs.ON-resistance non-linearly decreases with Vgs.Ans: 4) ON-resistance non-linearly decreases with Vgs.12. State True or FalseStatement: Dynamic CMOS logic operates using two non-overlapping clock pulses.Solution: (2). What is the relation between the equivalent resistance of a switched capacitor and the capacitance?The resistance is proportional to the capacitance.The resistance is inversely proportional to the capacitance.The resistance is proportional to the square of the capacitance.The resistance is inversely proportional to the square of the capacitance.Ans: 2) The resistance is inversely proportional to the capacitance.32. What is system Verilog? What is the minimum number of transistors needed to design an XOR gate?Ans: 4) Six39. What is the use of CAD tools in VLSI design?It automates the VLSI design.It reduces the design cycle time.It reduces the chance of errors.All of the above.Ans: 4) All of the above.6. Which type of product is more suitable for FPGA based Design?Large scale product development.High Speed applications.Prototype development.Low power applications.Ans: 3) Prototype development.What is Verilog? On which factors, the power dissipation of a CMOS inverter depends?Supplied Voltage.NMOSFET’s channel width.PMOSFET’s channel width.All of the above.Ans: 1) Supplied Voltage22. State True or FalseStatement: A current mirror circuit can be used as a current amplifier by increasing the (W/L) ratios of the mirrored and source MOSFETSolution: (1). True29. How does power dissipation occur for full scaling?Increases by a factor of sIncreases by a factor of s2.Decreases by a factor for s.Decreases by a factor for s2.Ans: 3) Decreases by a factor of s2.16. What is the number of Metal Oxide Filed Effect Transistors are needed to construct a Bi-complementary metal Oxide Semiconductor NOR gate which have two input?5 MOSFETs6 MOSFETs7 MOSFETs8 MOSFETsAns: 3) 7 MOSFETs“How a Logic gate is designed in VLSI?” Find the answer here!3. True36. These isbecause we the Wisdomjobs will provide you withthe complete details about the interview questionand answers and also, we will provide the differentjobs roles to apply easily. Which of the following is true about VLSI logic design?VLSI minimizes the area and delayVLSI minimizes the area at the cost of delayVLSI maximizes speed by decreasing areaVLSI minimizes delay by reducing the areaAns: 2) VLSI minimizes the area at the cost of delay.27. State True or FalseStatement: The PMOS transistors act as Pull-up network in a CMOS inverter.Solution: (1). Find the odd one out.Channel length modulationSubthreshold ConductionHot carrier effect.Body EffectAns: 4) Body effect. Which connections of NMOS in PDN, help to realize the AND terms?Cascade ConnectionAnti – parallel ConnectionsSeries ConnectionsParallel ConnectionsAns: 3) Series Connections37. Which type of logic design provides the minimum propagation delay?Emitter Coupled LogicTransistor Transistor LogicRegister Transistor LogicDiode Transistor LogicAns: 1) Emitter Coupled Logic40. To clear any interview, one must work hard toclear it in first attempt. True20. So simply to save your timewe have provided all the necessary details aboutVHDL Interview Questions and Answers and VHDLjobs at one place.VHDL INTERVIEW QUESTIONS &ANSWERSΞ(VLSI, Verilog Interview Questions, Image Credit – Google PlayVery High Definition LanguageVery High Speed Integration Hardware Description LanguageVery High Description LanguageVery High Speed Scaling Hardware Describing LanguageAns: 2) Very High Speed Integration Hardware Description LanguageFor basic VHDL Tutorials, Click Here!2. Where does the subthreshold operation of MOSFET find applications?Memories.Charge coupled devices.Biomedical applications.None of the above.Ans: 3) Biomedical applications.Make your First VHDL Project!Click Here!VLSI, VHDL, Verilog Interview Questions, Image – 111. What is the threshold voltage of an EMOSFET?Equal to 0 V.Less than 0 V.Greater than 0 V.None of the above.Ans: 3) Greater than 0 V.13. What is the relation between the equivalent resistance of a switched capacitor and the clock frequency?The resistance is proportional to clock frequency.The resistance is inversely proportional to clock frequency.The resistance is proportional to the square of the clock frequency.The resistance is inversely proportional to the square of the clock frequency.Ans: 2) The resistance is inversely proportional to clock frequency.30 Most important and frequently asked VLSI Interview Questions! Click Here!VLSI, VHDL, Verilog Interview Questions, Image – 331. Which is true about VLSI design?VLSI is a sequential process which has feedback loops.VLSI is a parallel process which has no feedback loops.VLSI is both sequential and parallel process that has feedback loops.VLSI is a sequential process which has no feedback loops.Ans: 3) VLSI is both sequential and parallel process that has feedback loops.For more details about Verilog Interview Questions and other topic like VLSI Design, Check this!5. What is the condition for domination by Drift Current?Strong InversionWeak InversionBoth Strong and weak inversion.Cannot be determined.Ans: 1) Strong Inversion.34. Which type of transistor can pass logic-high value perfectly, but not the logic-low value?NMOSFETPMOSFETCMOSNone of the aboveAns: 2) PMOSFET38. and other Verilog Interview Questions and Answers are here!7. VHDL aremuch in demand. False9. There are various leadingcompanies that offer jobs in various roles like RTLVerification Engineer - VHDL/SystemC, Vlsi Jobs inHyderabad, Digilogic Systems - FPGA Engineer -Verilog/RTL Design/Synthesis many other rolestoo. How does power dissipation occur for constant voltage scaling?Increases by a factor of sIncreases by a factor of s2.Decreases by a factor for s.Decreases by a factor for s2.Ans: 1) Increases by a factor of s.17. How does doping density change for constant voltage scaling?Increases by a factor of sIncreases by a factor of s2.Decreases by a factor for s.Decreases by a factor for s2.Ans: 2) Increases by a factor of s2.15. What is the equivalent circuit for CMOS comparator?Uncompensated CMOS OPAMP.Compensated CMOS OPAMP.Partially Compensated CMOS OPAMP.None of the above is true.Ans: 1) Uncompensated CMOS OPAMP.30. Why does lowest propagation delay occur through a gate?Due to – strong transistor, high temperature, high voltage.Due to – strong transistor, low temperature, high voltage.Due to – Weak transistor, high temperature, high voltage.Due to – weak transistor, low temperature, low voltage.Ans: 3) Due to – Weak transistor, high temperature, high voltage.26. State True or FalseStatement: In full scaling, the magnitude of the electric field is constant.Solution: (1). False.For more VLSI related topic and Verilog interview questions click here State True or FalseStatement: The full form of SPICE is – Simulation Program with Integrated Circuit Emphasis.Solution: (1). What is a hard macro?Flexible BlockFixed BlockFlexible block with a fixed aspect ratioFlexible block with a flexible aspect ratioAns: 2) Fixed Block28. State True or FalseStatement: In the cascode current mirror, the output resistance is increased.Solution: (1). What is the effect of ‘Delay’ if the power supply voltage gets increased? IncreasesDecreasesRemains the sameDelay has nothing o do with power supply.Ans: 2) Decreases4. True23. What does the ASIC cell library contain?The physical layout of the cellsRouting model of the cellsTiming model of the cellsAll of the above.Ans: 1) Physical layout of the cells.25. Why a short channel device is preferred?It is easier for fabrication.It has lower power consumption.It has high speed.It has better output characteristics.Ans: 3) It has high speed.10. Which of the following effect has no contribution to deviate the ideal situation of a current mirror circuit?DIBL effects.Threshold offset between two transistorsChannel length modulationImperfect geometrical matching.Ans: 1) DIBL effects.24. (All the other options are 2nd order effect).14. What is the main advantage of depletion load NMOSFET inverter over EMOSFET load?Less power dissipationEasier fabrication processSharper Vtc transitions and better noise margins.None of the above.Ans: 3) Sharper Vtc transitions and better noise margin.18. Why our jobs site is easy for anyone to learn and tocrack interview in the first attempt? True35. The full form of VHDL isVHSIC Hardware Description Language. What is the relation between interconnect delay and gate delay?The Relation is technology dependent.Gate delay always more than interconnect delay.Interconnect delay always more than the gate delay.They are same.Ans: 1) The relation is technology dependent.8. State True or FalseStatement: For a Y chart, the details of design information increases when moved from the centre to the periphery.Ans: (2). Why is polysilicon used for the gate in MOSFET?Because it is a semi-metal.Because it has lattice matching with SiliconeBecause it is easier to fabricate.None of the above.Ans: 2) Because it has lattice matching with silicone.19. What is the condition for domination by Diffusion Current?Strong InversionWeak InversionBoth Strong and weak inversion.Cannot be determined.Ans: 2) Weak Inversion.33. Which of the given statement is true regarding a MOSFET inverter?One PMOSFET and one resistor are needed to implement a MOSFET inverter.One NMOSFET and one resistor are needed to implement a MOSFET inverter.Two PMOSFETs.Two NMOSFETs.Ans: 2) One NMOSFET and one resistor is needed to implement a MOSFET inverter.Build your first Verilog project!Click here!VLSI, VHDL, Verilog Interview Questions, Image – 221.

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